



# PCF8563

Real-time clock/calendar

Rev. 06 — 21 February 2008

Product data sheet

## 1. General description

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The PCF8563 is a CMOS real-time clock/calendar optimized for low power consumption. A programmable clock output, interrupt output and voltage-low detector are also provided. All addresses and data are transferred serially via a two-line bidirectional I<sup>2</sup>C-bus. Maximum bus speed is 400 kbit/s. The built-in word address register is incremented automatically after each written or read data byte.

## 2. Features

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- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Century flag
- Clock operating voltage: 1.8 V to 5.5 V
- Low backup current; typical 0.25  $\mu$ A at  $V_{DD} = 3.0$  V and  $T_{amb} = 25$  °C
- 400 kHz two-wire I<sup>2</sup>C-bus interface (at  $V_{DD} = 1.8$  V to 5.5 V)
- Programmable clock output for peripheral devices (32.768 kHz, 1024 Hz, 32 Hz and 1 Hz)
- Alarm and timer functions
- Integrated oscillator capacitor
- Internal power-on reset
- I<sup>2</sup>C-bus slave address: read A3h and write A2h
- Open-drain interrupt pin
- ElectroStatic Discharge (ESD) protection exceeds 2000 V Human Body Model (HBM) per JESD22-A114, 200 V Machine Model (MM) per JESD22-A115 and 2000 V Charged Device Model (CDM) per JESD22-C101
- Latch-up testing is done to JEDEC standard JESD78 which exceeds 100 mA

## 3. Applications

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- Mobile telephones
- Portable instruments
- Electronic metering
- Battery powered products

### 4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		Version
		Name	Description	
PCF8563P	PCF8563P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PCF8563T	8563T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCF8563TS	8563	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCF8563BS	8563S	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm	SOT650-1

### 5. Block diagram

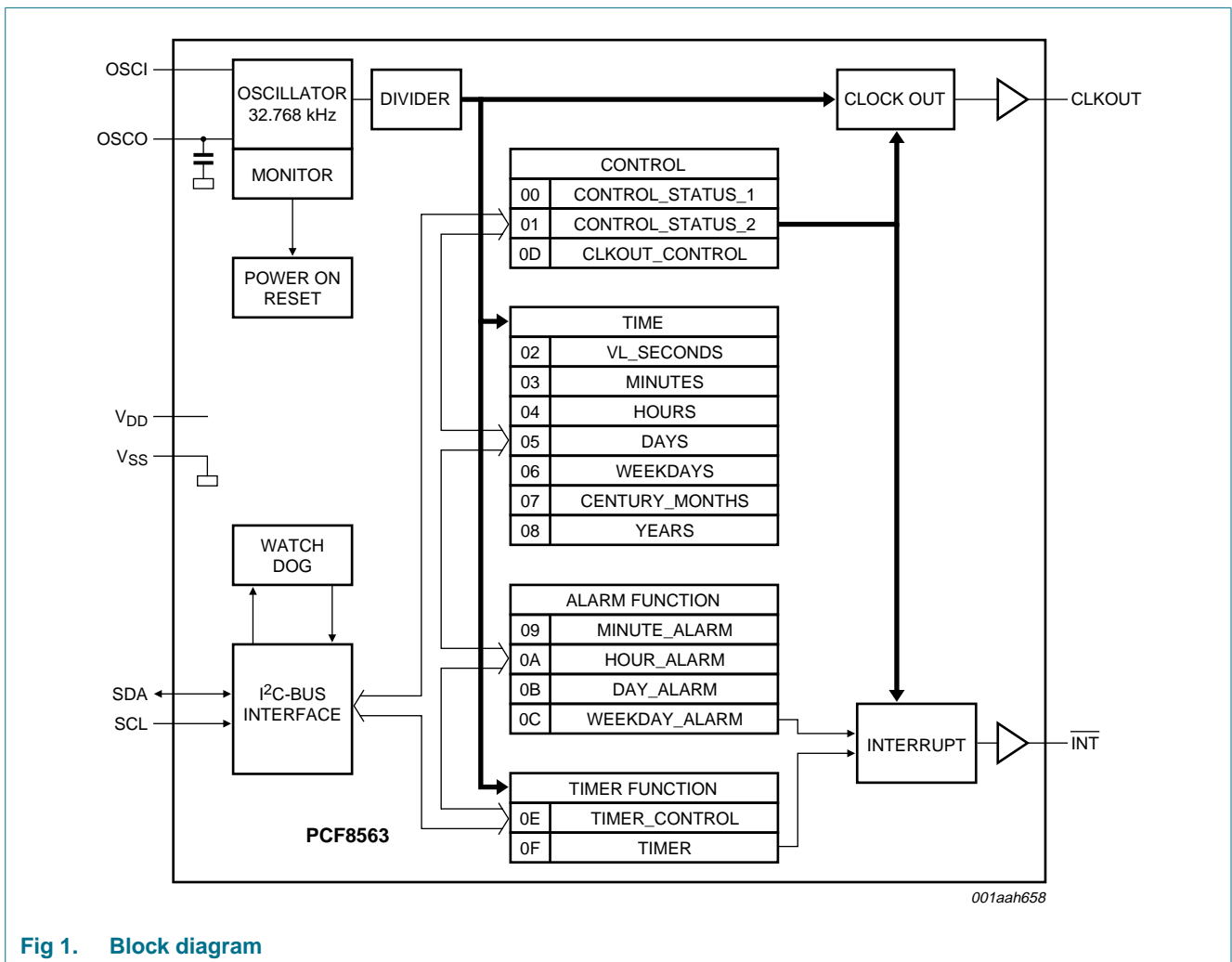
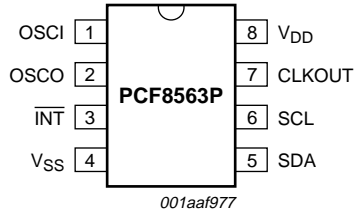


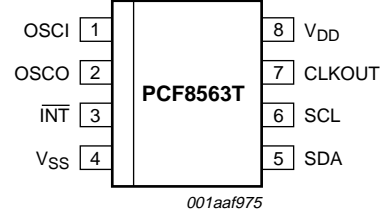
Fig 1. Block diagram

## 6. Pinning information

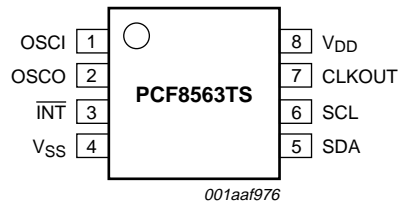
### 6.1 Pinning



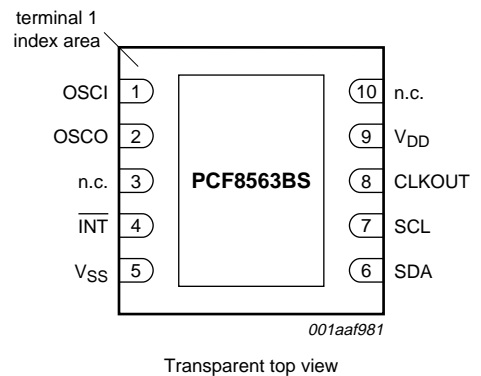
**Fig 2. Pin configuration DIP8**



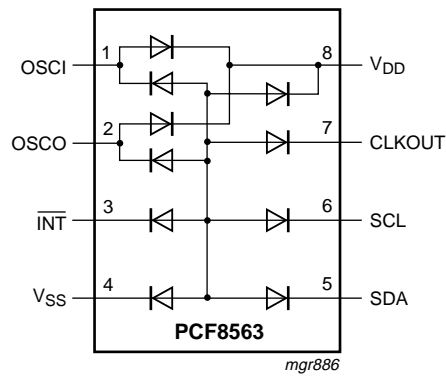
**Fig 3. Pin configuration SO8**



**Fig 4. Pin configuration TSSOP8**



**Fig 5. Pin configuration HVSON10**



**Fig 6. Device diode protection diagram**

## 6.2 Pin description

Table 2. Pin description

Symbol	Pin		Description
	DIP8, SO8, TSSOP8	HVSON10	
OSCI	1	1	oscillator input
OSCO	2	2	oscillator output
n.c.	-	3	not connected
$\overline{\text{INT}}$	3	4	interrupt output (open-drain; active LOW)
V <sub>SS</sub>	4	5	ground
SDA	5	6	serial data input and output
SCL	6	7	serial clock input
CLKOUT	7	8	clock output, open-drain
V <sub>DD</sub>	8	9	positive supply voltage
n.c.	-	10	not connected

## 7. Functional description

The PCF8563 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock/calendar (RTC), a programmable clock output, a timer, an alarm, a voltage-low detector and a 400 kHz I<sup>2</sup>C-bus interface.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented. The first two registers (memory address 00h and 01h) are used as control and/or status registers. The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years counters). Address locations 09h through 0Ch contain alarm registers which define the conditions for an alarm. Address 0Dh controls the CLKOUT output frequency. 0Eh and 0Fh are the timer control and timer registers, respectively.

The seconds, minutes, hours, days, weekdays, months, years as well as the minute alarm, hour alarm, day alarm and weekday alarm registers are all coded in Binary Coded Decimal (BCD) format.

When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.

### 7.1 Alarm function modes

By clearing the MSB of one or more of the alarm registers (bit AE = Alarm Enable), the corresponding alarm condition(s) will be active. In this way an alarm can be generated from once per minute up to once per week. The alarm condition sets the Alarm Flag (AF). The asserted AF can be used to generate an interrupt (on pin  $\overline{\text{INT}}$ ). The AF can only be cleared by software.

### 7.2 Timer

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or  $\frac{1}{60}$  Hz), and enables or disables the timer. The timer counts down from a software-loaded 8-bit binary value. At the end of every countdown, the timer sets the Timer Flag (TF). The TF may only be cleared by software. The asserted TF can be used to generate an interrupt (on pin  $\overline{INT}$ ). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the state of TF. Bit TI\_TP is used to control this mode selection. When reading the timer, the current countdown value is returned.

### 7.3 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the CLKOUT control register at address 0Dh. Frequencies of 32.768 kHz (default), 1024 Hz, 32 Hz and 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator. CLKOUT is an open-drain output and enabled at power-on. If disabled it becomes high-impedance.

### 7.4 Reset

The PCF8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I<sup>2</sup>C-bus logic is initialized and all registers are reset according to [Table 25](#).

### 7.5 Voltage-low detector

The PCF8563 has an on-chip voltage-low detector (see [Figure 7](#)). When  $V_{DD}$  drops below  $V_{low}$ , bit VL in the seconds register is set to indicate that the integrity of the clock information is no longer guaranteed. The VL flag can only be cleared by software.

Bit VL is intended to detect the situation when  $V_{DD}$  is decreasing slowly, for example under battery operation. Should  $V_{DD}$  reach  $V_{low}$  before power is re-asserted then bit VL is set. This will indicate that the time may be corrupted.

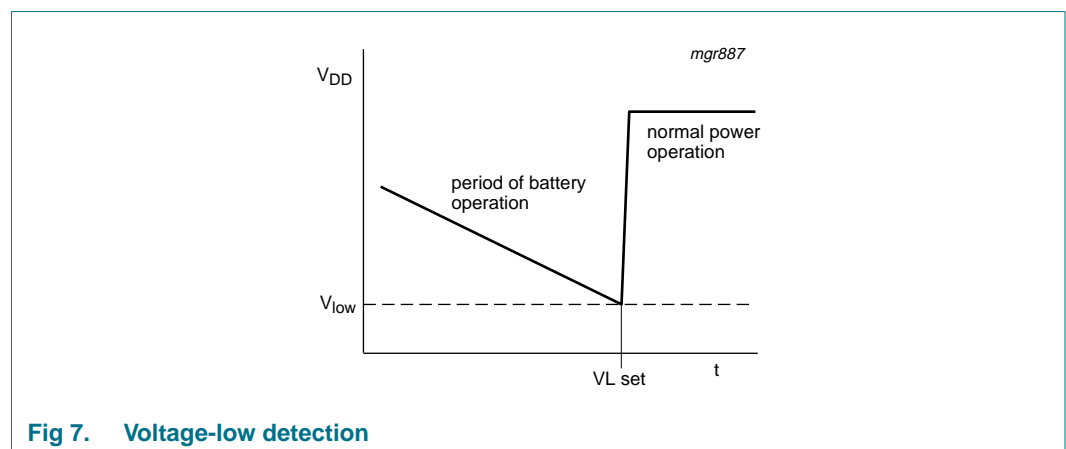


Fig 7. Voltage-low detection

### 7.6 Register organization

**Table 3. Formatted registers overview**

Bit positions labelled as x are not relevant. Bit positions labelled with 0 should always be written with logic 0; if read they could be either logic 0 or logic 1.

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	control_status_1	TEST1	0	STOP	0	TESTC	0	0	0
01h	control_status_2	0	0	0	TI_TP	AF	TF	AIE	TIE
02h	VL_seconds	VL	<seconds 00 to 59 coded in BCD>						
03h	minutes	x	<minutes 00 to 59 coded in BCD>						
04h	hours	x	x	<hours 00 to 23 coded in BCD>					
05h	days	x	x	<days 01 to 31 coded in BCD>					
06h	weekdays	x	x	x	x	x	<weekdays 0 to 6 in BCD>		
07h	century_months	C	x	x	<months 01 to 12 coded in BCD>				
08h	years	<years 00 to 99 coded in BCD>							
09h	minute_alarm	AE	<minute alarm 00 to 59 coded in BCD>						
0Ah	hour_alarm	AE	x	<hour alarm 00 to 23 coded in BCD>					
0Bh	day_alarm	AE	x	<day alarm 01 to 31 coded in BCD>					
0Ch	weekday_alarm	AE	x	x	x	x	<weekday alarm 0 to 6 in BCD>		
0Dh	CLKOUT_control	FE	x	x	x	x	x	FD1	FD0
0Eh	timer_control	TE	x	x	x	x	x	TD1	TD0
0Fh	timer	<timer countdown value>							

#### 7.6.1 Control\_status\_1 register

**Table 4. Control\_status\_1 - Control and Status register 1 (address 00h) bit description**

Bit	Symbol	Value	Description
7	TEST1	0	Normal mode
		1	EXT_CLK test mode
6	0	default value is logic 0	
5	STOP	0	RTC source clock runs
		1	all RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz is still available)
4	0	default value is logic 0	
3	TESTC	0	Power-on reset override facility is disabled; set to logic 0 for normal operation
		1	Power-on reset override may be enabled
2 to 0	0	default value is logic 0	

#### 7.6.2 Control\_status\_2 register

Bits TF and AF: When an alarm occurs, AF is set to logic 1. Similarly, at the end of a timer countdown, TF is set to logic 1. These bits maintain their value until overwritten by software. If both timer and alarm interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logic AND is performed during a write access.

Bits TIE and AIE: These bits activate or deactivate the generation of an interrupt when TF or AF is asserted, respectively. The interrupt is the logical OR of these two conditions when both AIE and TIE are set.

**Table 5. Control\_status\_2 - Control and Status register 2 (address 01h) bit description**

Bit	Symbol	Value	Description
7 to 5	0		default value is logic 0
4	TI_TP	0	$\overline{\text{INT}}$ is active when TF is active (subject to the status of TIE)
		1	$\overline{\text{INT}}$ pulses active according to Table 6 (subject to the status of TIE); note that if AF and AIE are active then $\overline{\text{INT}}$ will be permanently active
3	AF	0 (read)	alarm flag inactive
		1 (read)	alarm flag active
		0 (write)	alarm flag is cleared
		1 (write)	alarm flag remains unchanged
2	TF	0 (read)	timer flag inactive
		1 (read)	timer flag active
		0 (write)	timer flag is cleared
		1 (write)	timer flag remains unchanged
1	AIE	0	alarm interrupt disabled
		1	alarm interrupt enabled
0	TIE	0	timer interrupt disabled
		1	timer interrupt enabled

**Table 6.  $\overline{\text{INT}}$  operation (bit TI\_TP = 1)**

Source clock (Hz)	$\overline{\text{INT}}$ period (s) <sup>[1]</sup>	
	n = 1 <sup>[2]</sup>	n > 1 <sup>[2]</sup>
4096	$\frac{1}{8192}$	$\frac{1}{4096}$
64	$\frac{1}{128}$	$\frac{1}{64}$
1	$\frac{1}{64}$	$\frac{1}{64}$
$\frac{1}{60}$	$\frac{1}{64}$	$\frac{1}{64}$

[1] TF and  $\overline{\text{INT}}$  become active simultaneously.

[2] n = loaded countdown value. Timer stopped when n = 0.

### 7.6.3 Time and date registers

**Table 7. VL\_seconds - Validity and Seconds register (address 02h) bit description**

Bit	Symbol	Value	Description
7	VL	0	clock integrity is guaranteed
		1	integrity of the clock information is no longer guaranteed
6 to 0	SECONDS[6:0]	00 to 59	the current seconds, coded in BCD format. Example: seconds register contains x101 1001 = 59 seconds

**Table 8. Minutes - Minutes register (address 03h) bit description**

Bit	Symbol	Value	Description
7	x		not relevant
6 to 0	MINUTES[6:0]	00 to 59	the current minutes, coded in BCD format

**Table 9. Hours - Hours register (address 04h) bit description**

Bit	Symbol	Value	Description
7 to 6	x		not relevant
5 to 0	HOURS[5:0]	00 to 23	the current hours, coded in BCD format

**Table 10. Days - Days register (address 05h) bit description**

Bit	Symbol	Value	Description
7 to 6	x		not relevant
5 to 0	DAYS[5:0]	01 to 31	the current day, coded in BCD format <sup>[1]</sup>

[1] The PCF8563 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

**Table 11. Weekdays - Weekdays register (address 06h) bit description**

Bit	Symbol	Value	Description
7 to 3	x		not relevant
2 to 0 <sup>[1]</sup>	WEEKDAYS[2:0]	0 to 6	the current weekday, coded in BCD format, see <a href="#">Table 12</a> .

[1] These bits may be re-assigned by the user.

**Table 12. Weekday assignments**

Weekday	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	x	x	x	x	x	0	0	0
Monday	x	x	x	x	x	0	0	1
Tuesday	x	x	x	x	x	0	1	0
Wednesday	x	x	x	x	x	0	1	1
Thursday	x	x	x	x	x	1	0	0
Friday	x	x	x	x	x	1	0	1
Saturday	x	x	x	x	x	1	1	0

**Table 13. Century\_months - Century and Months register (address 07h) bit description**

Bit	Symbol	Value	Description
7	C <sup>[1]</sup>		century; this bit is toggled when the years register overflows from 99 to 00
		0	indicates the century is 20xx
		1	indicates the century is 19xx
6 to 5	x		not relevant
4 to 0	MONTHS[4:0]	01 to 12	the current month, coded in BCD format, see <a href="#">Table 14</a>

[1] This bit may be re-assigned by the user.



**Table 14. Month assignments**

Month	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	C	x	x	0	0	0	0	1
February	C	x	x	0	0	0	1	0
March	C	x	x	0	0	0	1	1
April	C	x	x	0	0	1	0	0
May	C	x	x	0	0	1	0	1
June	C	x	x	0	0	1	1	0
July	C	x	x	0	0	1	1	1
August	C	x	x	0	1	0	0	0
September	C	x	x	0	1	0	0	1
October	C	x	x	1	0	0	0	0
November	C	x	x	1	0	0	0	1
December	C	x	x	1	0	0	1	0

**Table 15. Years - Years register (address 08h) bit description**

Bit	Symbol	Value	Description
7 to 0	YEARS[7:0]	00 to 99	the current year, coded in BCD format

### 7.6.4 Alarm registers

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their bit AE at logic 1 will be ignored.

**Table 16. Minute\_alarm - Minute alarm register (address 09h) bit description**

Bit	Symbol	Value	Description
7	AE	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	ALARM_MINUTES[6:0]	00 to 59	the minute alarm information, coded in BCD format

**Table 17. Hour\_alarm - Hour alarm register (address 0Ah) bit description**

Bit	Symbol	Value	Description
7	AE	0	hour alarm is enabled
		1	hour alarm is disabled
6	x		not relevant
5 to 0	ALARM_HOURS[5:0]	00 to 23	the hour alarm information, coded in BCD format

**Table 18. Day\_alarm - Day alarm register (address 0Bh) bit description**

Bit	Symbol	Value	Description
7	AE	0	day alarm is enabled
		1	day alarm is disabled
6	x		not relevant
5 to 0	ALARM_DAYS[5:0]	01 to 31	the day alarm information, coded in BCD format

**Table 19. Weekday\_alarm - Weekday alarm register (address 0Ch) bit description**

Bit	Symbol	Value	Description
7	AE	0	weekday alarm is enabled
		1	weekday alarm is disabled
6 to 3	x		not relevant
2 to 0	ALARM_WEEKDAYS[2:0]	0 to 6	the weekday alarm information, coded in BCD format

### 7.6.5 Clock output control register

**Table 20. CLKOUT\_control - CLKOUT control register (address 0Dh) bit description**

Bit	Symbol	Value	Description
7	FE	0	the CLKOUT output is inhibited and set to high-impedance
		1	the CLKOUT output is activated
6 to 2	x		not relevant
1 to 0	FD[1:0]	see <a href="#">Table 21</a>	these bits control the frequency output at pin CLKOUT

**Table 21. FD1 and FD0: CLKOUT frequency selection**

FD1	FD0	CLKOUT frequency
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

### 7.6.6 Countdown timer

The timer register is an 8-bit binary countdown timer. It is enabled and disabled via the timer control register bit TE. The source clock for the timer is also selected by the timer control register. Other timer properties such as interrupt generation are controlled via control\_status\_2 register.

For accurate read back of the countdown value, the I<sup>2</sup>C-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock.

**Table 22. Timer\_control - Timer control register (address 0Eh) bit description**

Bit	Symbol	Value	Description
7	TE	0	timer is disabled
		1	timer is enabled
6 to 2	x		not relevant
1 to 0	TD[1:0]	see <a href="#">Table 23</a>	timer source clock frequency select; these bits determine the source clock for the countdown timer; when not in use, TD[1:0] should be set to 11 (1/60 Hz) for power saving

**Table 23. TD1 and TD0: Timer frequency selection**

TD1	TD0	TIMER Source clock frequency
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

**Table 24. Timer - Timer value register (address 0Fh) bit description**

Bit	Symbol	Value	Description
7 to 0	TIMER	00h to FFh	countdown value = n; $CountdownPeriod = \frac{n}{SourceClockFrequency}$

## 7.7 EXT\_CLK test mode

A Test mode is available which allows for on-board testing. In such a mode it is possible to set up test conditions and control the operation of the RTC.

The Test mode is entered by setting bit TEST1 in control\_status\_1 register. Then pin CLKOUT becomes an input. The Test mode replaces the internal 64 Hz signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT will then generate an increment of one second.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a minimum period of 1000 ns. The internal 64 Hz clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2<sup>6</sup> divide chain called a pre-scaler. The pre-scaler can be set into a known state by using bit STOP. When bit STOP is set, the pre-scaler is reset to 0 (STOP must be cleared before the pre-scaler can operate again).

From a STOP condition, the first 1 second increment will take place after 32 positive edges on CLKOUT. Thereafter, every 64 positive edges will cause a one-second increment.

**Remark:** Entry into EXT\_CLK test mode is not synchronized to the internal 64 Hz clock. When entering the Test mode, no assumption as to the state of the pre-scaler can be made.

Operation example:

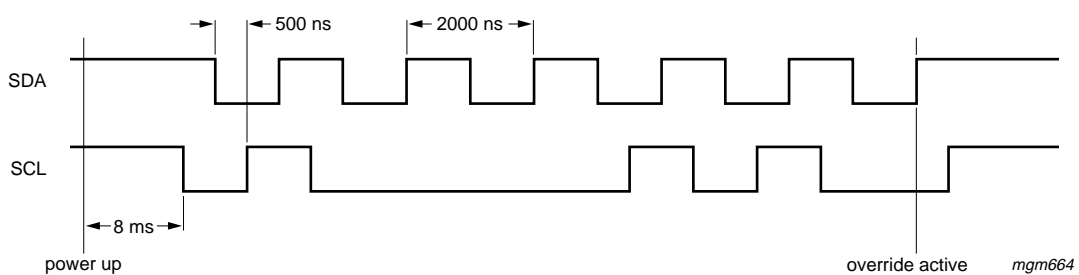
1. Set EXT\_CLK test mode (control\_status\_1, bit TEST1 = 1)
2. Set STOP (control\_status\_1, bit STOP = 1)
3. Clear STOP (control\_status\_1, bit STOP = 0)
4. Set time registers to desired value
5. Apply 32 clock pulses to CLKOUT
6. Read time registers to see the first change
7. Apply 64 clock pulses to CLKOUT
8. Read time registers to see the second change

Repeat steps 7 and 8 for additional increments.

### 7.8 Power-On Reset (POR) override

The POR duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up on-board test of the device. The setting of this mode requires that the I<sup>2</sup>C-bus pins, SDA and SCL, be toggled in a specific order as shown in [Figure 8](#). All timings are required minimums.

Once the Override mode has been entered, the device immediately stops being reset and normal operation may commence i.e. entry into the EXT\_CLK test mode via I<sup>2</sup>C-bus access. The Override mode may be cleared by writing a logic 0 to TESTC. TESTC must be set to logic 1 before re-entry into the Override mode is possible. Setting TESTC to logic 0 during normal operation has no effect except to prevent entry into the POR override mode.



**Fig 8.** POR override sequence

[Table 25](#) shows the register reset values.

**Table 25.** Register reset value<sup>[1]</sup>

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	control_status_1	0	0	0	0	1	0	0	0
01h	control_status_2	x	x	0	0	0	0	0	0
02h	VL_seconds	1	x	x	x	x	x	x	x
03h	minutes	1	x	x	x	x	x	x	x
04h	hours	x	x	x	x	x	x	x	x

Table 25. Register reset value<sup>[1]</sup> ...continued

Address	Register name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	days	x	x	x	x	x	x	x	x
06h	weekdays	x	x	x	x	x	x	x	x
07h	century_months	x	x	x	x	x	x	x	x
08h	years	x	x	x	x	x	x	x	x
09h	minute_alarm	1	x	x	x	x	x	x	x
0Ah	hour_alarm	1	x	x	x	x	x	x	x
0Bh	day_alarm	1	x	x	x	x	x	x	x
0Ch	weekday_alarm	1	x	x	x	x	x	x	x
0Dh	CLKOUT_control	1	x	x	x	x	x	0	0
0Eh	timer_control	0	x	x	x	x	x	1	1
0Fh	timer	x	x	x	x	x	x	x	x

[1] registers marked 'x' are undefined at power-up and unchanged by subsequent resets.

## 8. Characteristics of the I<sup>2</sup>C-bus

The I<sup>2</sup>C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

### 8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal (see [Figure 9](#)).

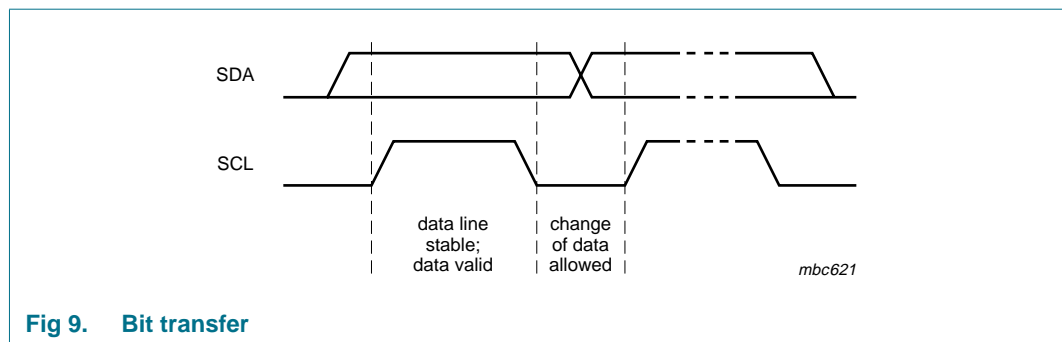


Fig 9. Bit transfer

### 8.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P); see [Figure 10](#).

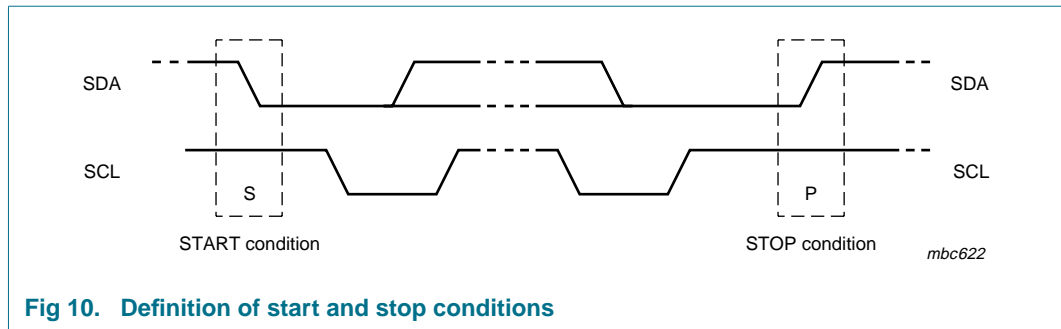


Fig 10. Definition of start and stop conditions

### 8.3 System configuration

A device generating a message is a transmitter, a device receiving a message is a receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see [Figure 11](#)).

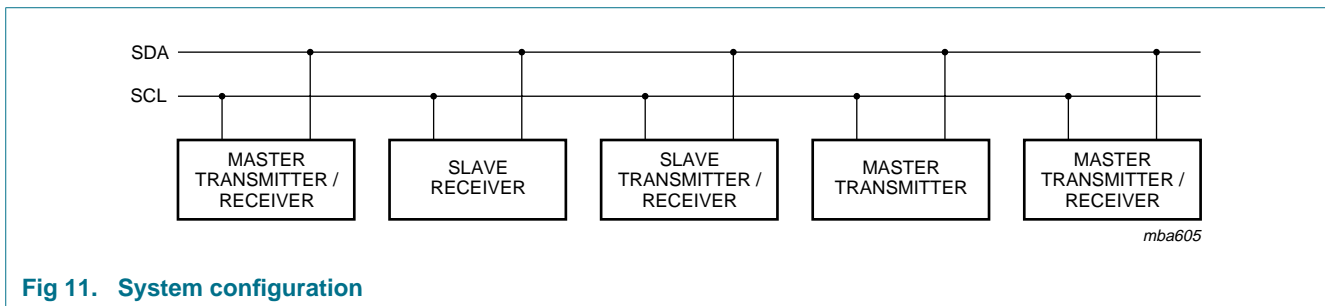


Fig 11. System configuration

### 8.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH-level signal put on the bus by the transmitter during which time the master generates an extra acknowledge-related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter (see [Figure 12](#)).

The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

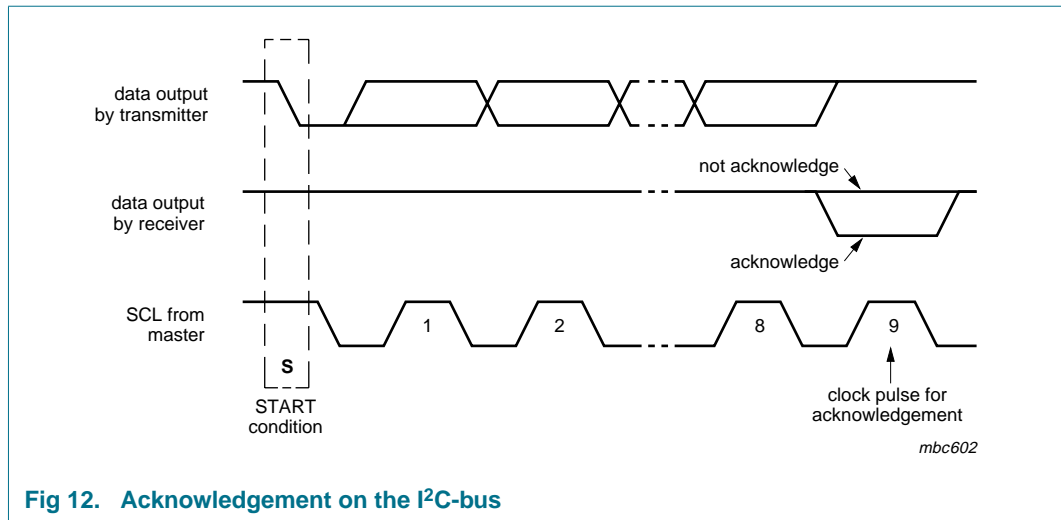


Fig 12. Acknowledgement on the I<sup>2</sup>C-bus

## 8.5 I<sup>2</sup>C-bus protocol

### 8.5.1 Addressing

Before any data is transmitted on the I<sup>2</sup>C-bus, the device which should respond is addressed first. The addressing is always carried out with the first byte transmitted after the start procedure.

The PCF8563 acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line.

The PCF8563 slave address is shown in [Figure 13](#).

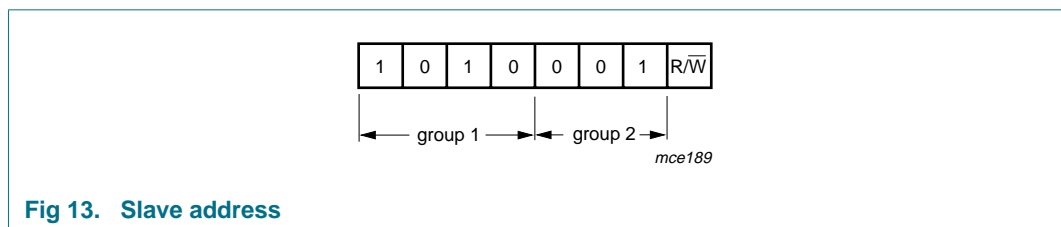


Fig 13. Slave address

### 8.5.2 Clock/calendar read/write cycles

The I<sup>2</sup>C-bus configuration for the different PCF8563 read and write cycles is shown in [Figure 14](#), [Figure 15](#) and [Figure 16](#). The word address is a 4-bit value that defines which register is to be accessed next. The upper four bits of the word address are not used.

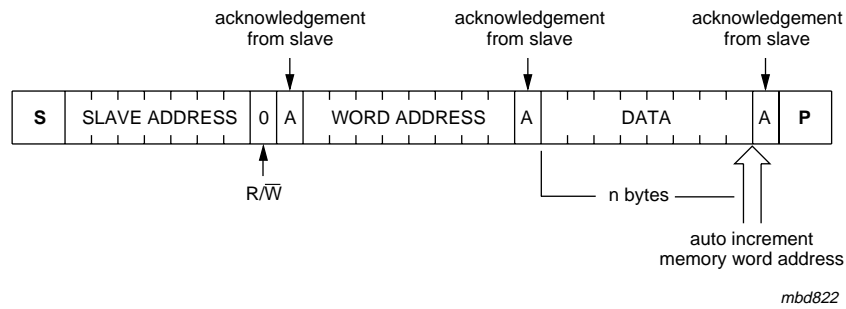


Fig 14. Master transmits to slave receiver (Write mode)

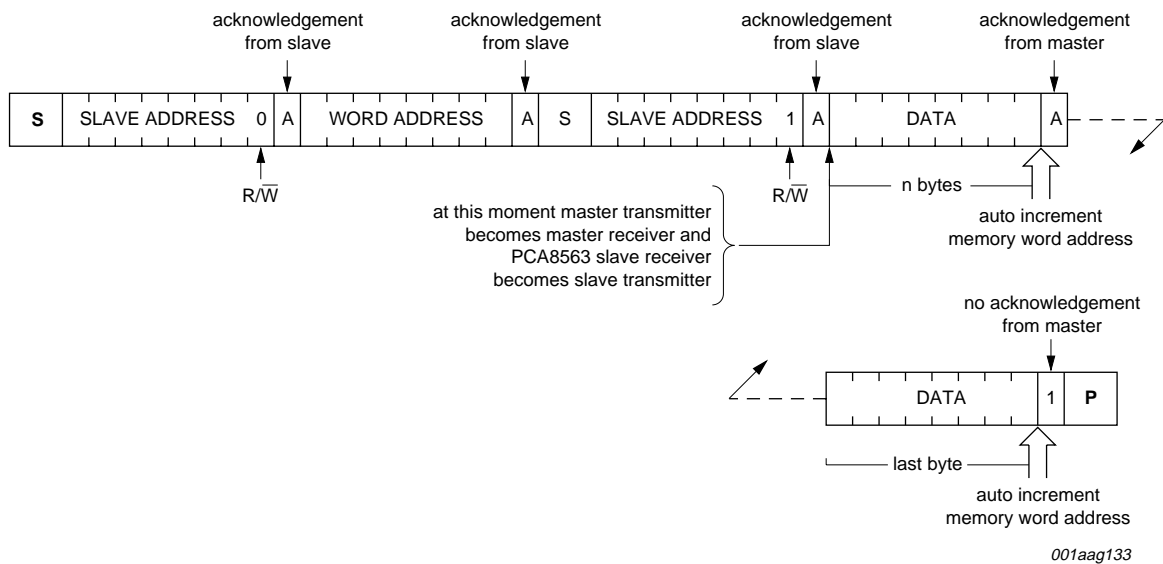


Fig 15. Master reads after setting word address (write word address; read data)

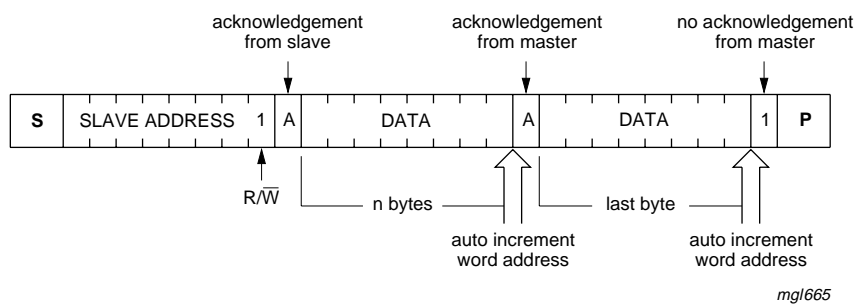


Fig 16. Master reads slave immediately after first byte (Read mode)



## 9. Limiting values

**Table 26. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.5	V
I <sub>DD</sub>	supply current		-50	+50	mA
V <sub>I</sub>	input voltage	on pins SCL and SDA	-0.5	+6.5	V
		on pin OSCI	-0.5	V <sub>DD</sub> + 0.5	V
V <sub>O</sub>	output voltage	on pins CLKOUT and $\overline{\text{INT}}$	-0.5	+6.5	V
I <sub>I</sub>	input current	at any input	-10	+10	mA
I <sub>O</sub>	output current	at any output	-10	+10	mA
P <sub>tot</sub>	total power dissipation		-	300	mW
T <sub>amb</sub>	ambient temperature		-40	+85	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C

## 10. Static characteristics

**Table 27. Static characteristics**

V<sub>DD</sub> = 1.8 V to 5.5 V; V<sub>SS</sub> = 0 V; T<sub>amb</sub> = -40 °C to +85 °C; f<sub>osc</sub> = 32.768 kHz; quartz R<sub>s</sub> = 40 kΩ; C<sub>L</sub> = 8 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
V <sub>DD</sub>	supply voltage	interface inactive; f <sub>SCL</sub> = 0 Hz; T <sub>amb</sub> = 25 °C; see <a href="#">Figure 20</a>	[1] 1.0	-	5.5	V
		interface active; f <sub>SCL</sub> = 400 kHz; see <a href="#">Figure 20</a>	[1] 1.8	-	5.5	V
		clock data integrity; T <sub>amb</sub> = 25 °C	V <sub>low</sub>	-	5.5	V
I <sub>DD</sub>	supply current	interface active; see <a href="#">Figure 19</a>				
		f <sub>SCL</sub> = 400 kHz	-	-	800	μA
		f <sub>SCL</sub> = 100 kHz	-	-	200	μA
		interface inactive (f <sub>SCL</sub> = 0 Hz); CLKOUT disabled; T <sub>amb</sub> = 25 °C; see <a href="#">Figure 17</a>	[2]			
		V <sub>DD</sub> = 5.0 V	-	275	550	nA
		V <sub>DD</sub> = 3.0 V	-	250	500	nA
		V <sub>DD</sub> = 2.0 V	-	225	450	nA
		interface inactive (f <sub>SCL</sub> = 0 Hz); CLKOUT disabled; T <sub>amb</sub> = -40 °C to +85 °C; see <a href="#">Figure 17</a>	[2]			
V <sub>DD</sub> = 5.0 V	-	500	750	nA		
V <sub>DD</sub> = 3.0 V	-	400	650	nA		
V <sub>DD</sub> = 2.0 V	-	400	600	nA		

**Table 27. Static characteristics ...continued**

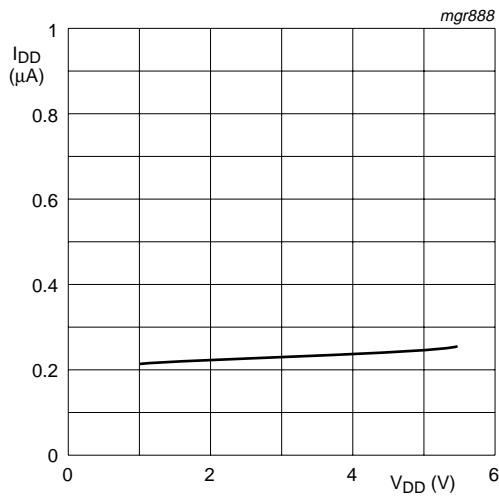
$V_{DD} = 1.8\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ;  $f_{osc} = 32.768\text{ kHz}$ ; quartz  $R_s = 40\text{ k}\Omega$ ;  $C_L = 8\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$I_{DD}$	supply current	interface inactive ( $f_{SCL} = 0\text{ Hz}$ ); CLKOUT enabled at 32 kHz; $T_{amb} = 25\text{ °C}$ ; see <a href="#">Figure 18</a>	[2]				
		$V_{DD} = 5.0\text{ V}$	-	825	1600	nA	
		$V_{DD} = 3.0\text{ V}$	-	550	1000	nA	
		$V_{DD} = 2.0\text{ V}$	-	425	800	nA	
		interface inactive ( $f_{SCL} = 0\text{ Hz}$ ); CLKOUT enabled at 32 kHz; $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; see <a href="#">Figure 18</a>	[2]				
		$V_{DD} = 5.0\text{ V}$	-	950	1700	nA	
	$V_{DD} = 3.0\text{ V}$	-	650	1100	nA		
	$V_{DD} = 2.0\text{ V}$	-	500	900	nA		
<b>Inputs</b>							
$V_{IL}$	LOW-level input voltage		$V_{SS}$	-	$0.3V_{DD}$	V	
$V_{IH}$	HIGH-level input voltage		$0.7V_{DD}$	-	$V_{DD}$	V	
$I_{LI}$	input leakage current	$V_I = V_{DD}$ or $V_{SS}$	-1	0	+1	$\mu\text{A}$	
$C_i$	input capacitance		[3]	-	7	pF	
<b>Outputs</b>							
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 5\text{ V}$					
		on pin SDA	-3	-	-	mA	
		on pin $\overline{\text{INT}}$	-1	-	-	mA	
		on pin CLKOUT	-1	-	-	mA	
$I_{OH}$	HIGH-level output current	on pin CLKOUT; $V_{OH} = 4.6\text{ V}$ ; $V_{DD} = 5\text{ V}$	1	-	-	mA	
$I_{LO}$	output leakage current	$V_O = V_{DD}$ or $V_{SS}$	-1	0	+1	$\mu\text{A}$	
<b>Voltage detector</b>							
$V_{low}$	low voltage	$T_{amb} = 25\text{ °C}$ ; sets bit VL; see <a href="#">Figure 7</a>	-	0.9	1.0	V	

[1] For reliable oscillator start-up at power-up:  $V_{DD(\text{min})\text{power-up}} = V_{DD(\text{min})} + 0.3\text{ V}$ .

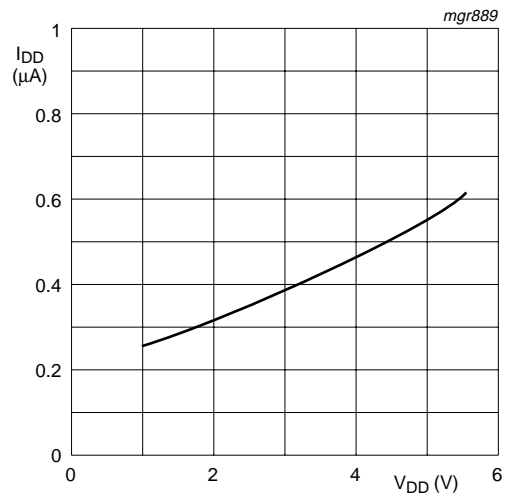
[2] Timer source clock =  $\frac{1}{60}\text{ Hz}$ , level of pins SCL and SDA is  $V_{DD}$  or  $V_{SS}$ .

[3] Tested on sample basis.



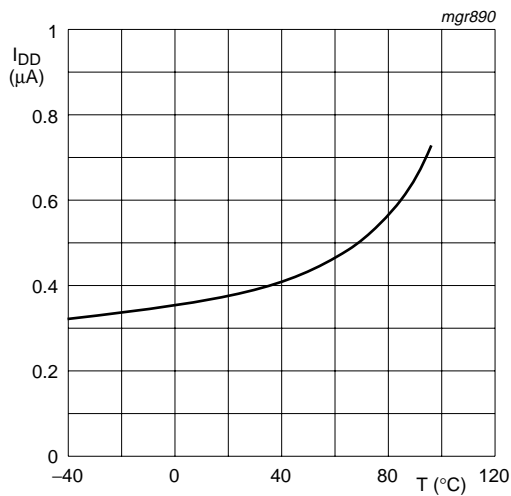
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; Timer = 1 minute.

**Fig 17.** Supply current  $I_{DD}$  as a function of supply voltage  $V_{DD}$ ; CLKOUT disabled



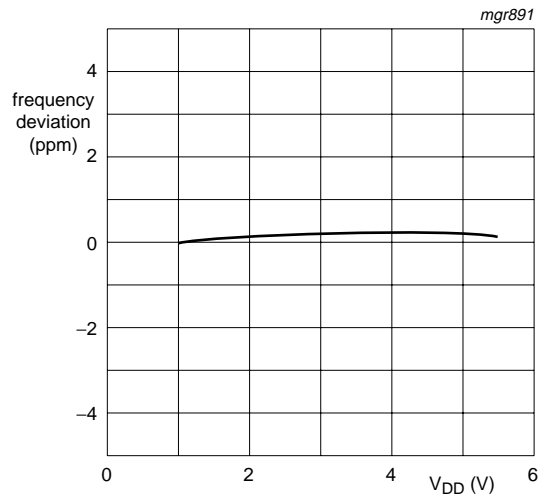
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; Timer = 1 minute.

**Fig 18.** Supply current  $I_{DD}$  as a function of supply voltage  $V_{DD}$ ; CLKOUT = 32 kHz



$V_{DD} = 3\text{ V}$ ; Timer = 1 minute.

**Fig 19.** Supply current  $I_{DD}$  as a function of temperature T; CLKOUT = 32 kHz



$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; normalized to  $V_{DD} = 3\text{ V}$ .

**Fig 20.** Frequency deviation as a function of supply voltage  $V_{DD}$

## 11. Dynamic characteristics

**Table 28. Dynamic characteristics**

$V_{DD} = 1.8\text{ V to }5.5\text{ V}$ ;  $V_{SS} = 0\text{ V}$ ;  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ;  $f_{osc} = 32.768\text{ kHz}$ ; quartz  $R_s = 40\text{ k}\Omega$ ;  $C_L = 8\text{ pF}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Oscillator</b>						
$C_{L(itg)}$	integrated load capacitance		15	25	35	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	$\Delta V_{DD} = 200\text{ mV}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	$2 \times 10^{-7}$	-	
<b>Quartz crystal parameters (f = 32.768 kHz)</b>						
$R_s$	series resistance		-	-	40	k $\Omega$
$C_L$	load capacitance	parallel	-	10	-	pF
$C_{trim}$	trimmer capacitance		5	-	25	pF
<b>CLKOUT output</b>						
$\delta_{CLKOUT}$	duty cycle on pin CLKOUT		[1]	50	-	%
<b>I<sup>2</sup>C-bus timing characteristics (see Figure 21)</b>						
$f_{SCL}$	SCL clock frequency		[4]	-	400	kHz
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	$\mu\text{s}$
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	$\mu\text{s}$
$t_{LOW}$	LOW period of the SCL clock		1.3	-	-	$\mu\text{s}$
$t_{HIGH}$	HIGH period of the SCL clock		0.6	-	-	$\mu\text{s}$
$t_r$	rise time of both SDA and SCL signals	SDA	-	-	0.3	$\mu\text{s}$
		SCL	-	-	0.3	$\mu\text{s}$
$t_f$	fall time of both SDA and SCL signals	SDA	-	-	0.3	$\mu\text{s}$
		SCL	-	-	0.3	$\mu\text{s}$
$C_b$	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	$\mu\text{s}$
$t_w(\text{spike})$	spike pulse width	on bus	-	-	50	ns

[1] Unspecified for  $f_{CLKOUT} = 32.768\text{ kHz}$ .

[2] All timing values are valid within the operating supply voltage at ambient temperature and referenced to  $V_{IL}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD}$ .

[3] A detailed description of the I<sup>2</sup>C-bus specification, with applications, is given in brochure *The I<sup>2</sup>C-bus specification*. This brochure may be ordered using the code 9398 393 40011.

[4] I<sup>2</sup>C-bus access time between two STARTs or between a START and a STOP condition to this device must be less than one second.

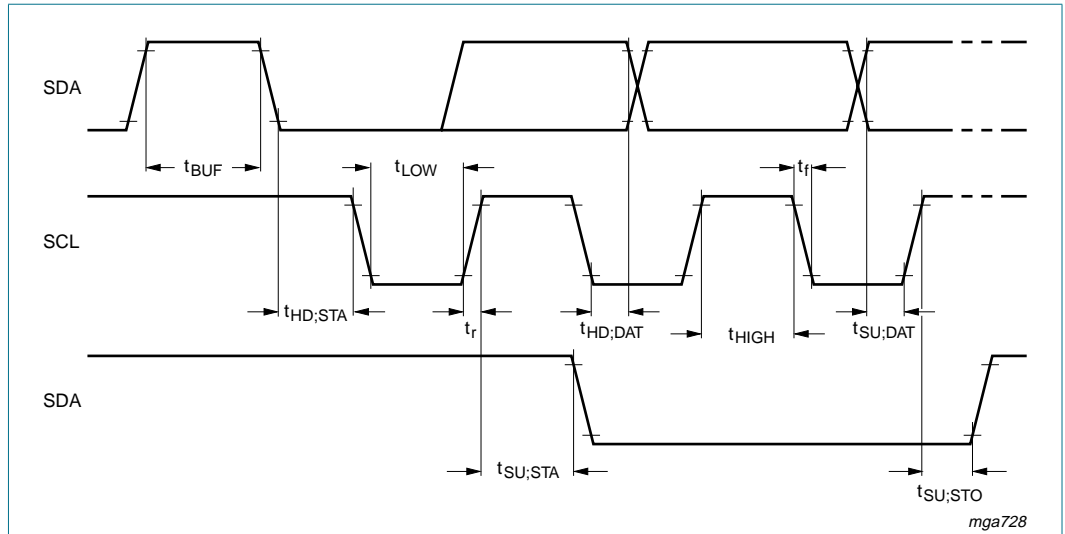


Fig 21. I<sup>2</sup>C-bus timing waveforms

## 12. Application information

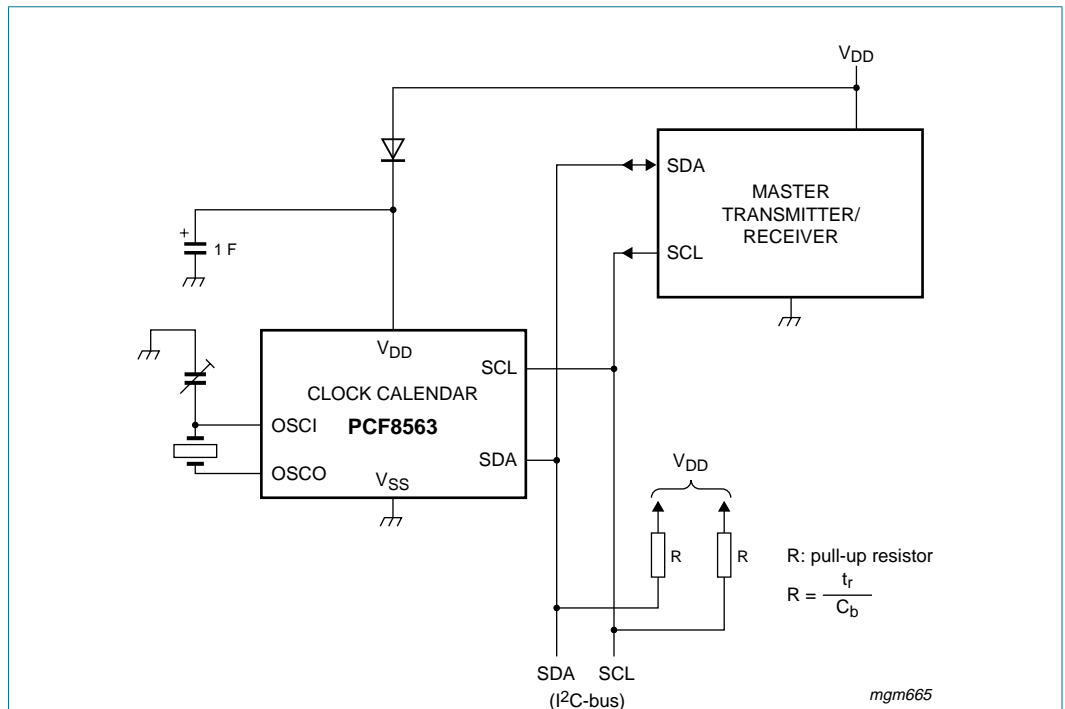


Fig 22. Application diagram

## 12.1 Quartz frequency adjustment

### 12.1.1 Method 1: fixed OSCI capacitor

By evaluating the average capacitance necessary for the application layout, a fixed capacitor can be used. The frequency is best measured via the 32.768 kHz signal available after power-on at pin CLKOUT. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average  $\pm 5 \times 10^{-6}$ ). Average deviations of  $\pm 5$  minutes per year can be easily achieved.

### 12.1.2 Method 2: OSCI trimmer

Using the 32.768 kHz signal available after power-on at pin CLKOUT, fast setting of a trimmer is possible.

### 12.1.3 Method 3: OSCO output

Direct measurement of OSCO out (accounting for test probe capacitance).

13. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

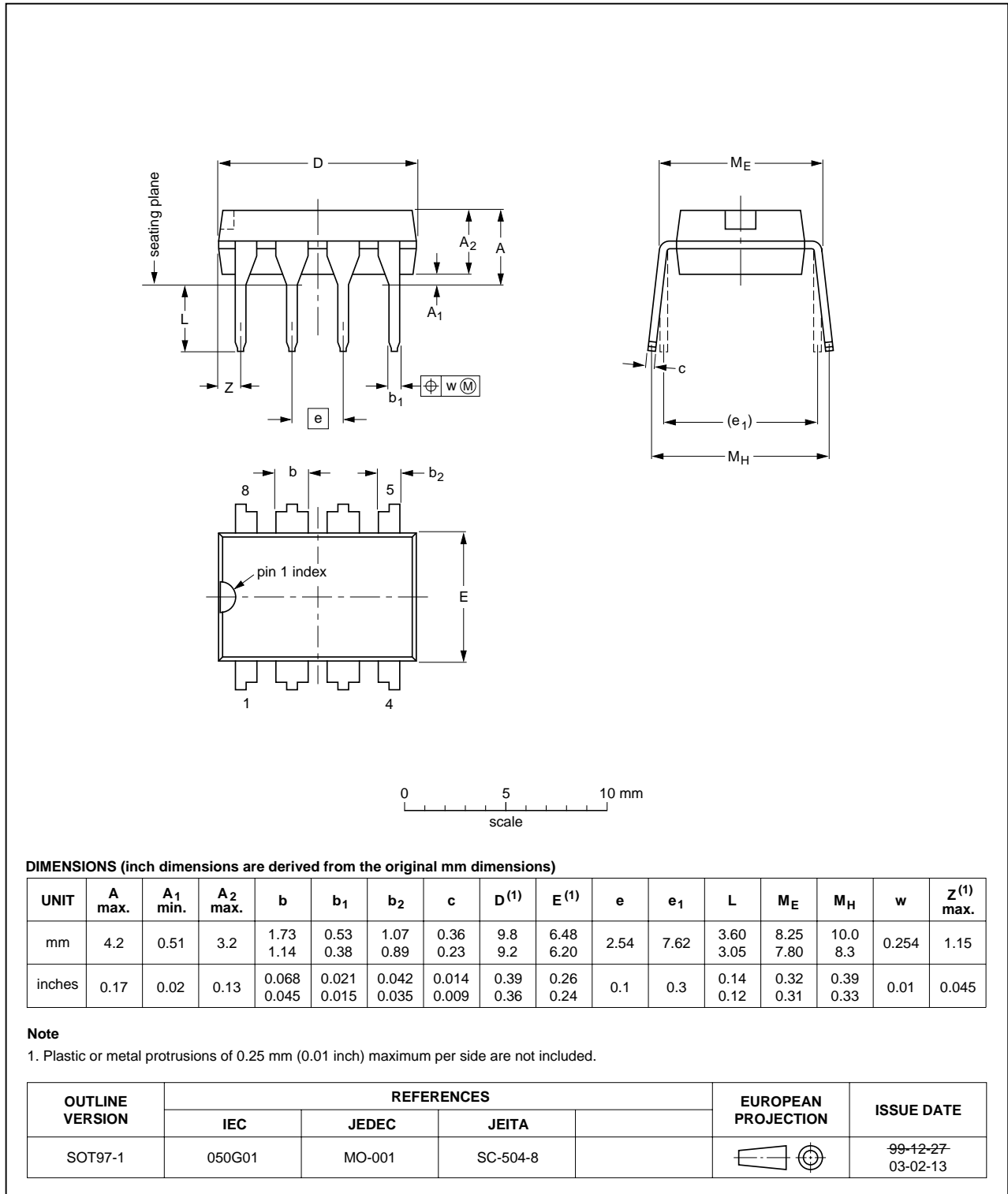


Fig 23. Package outline SOT97-1 (DIP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

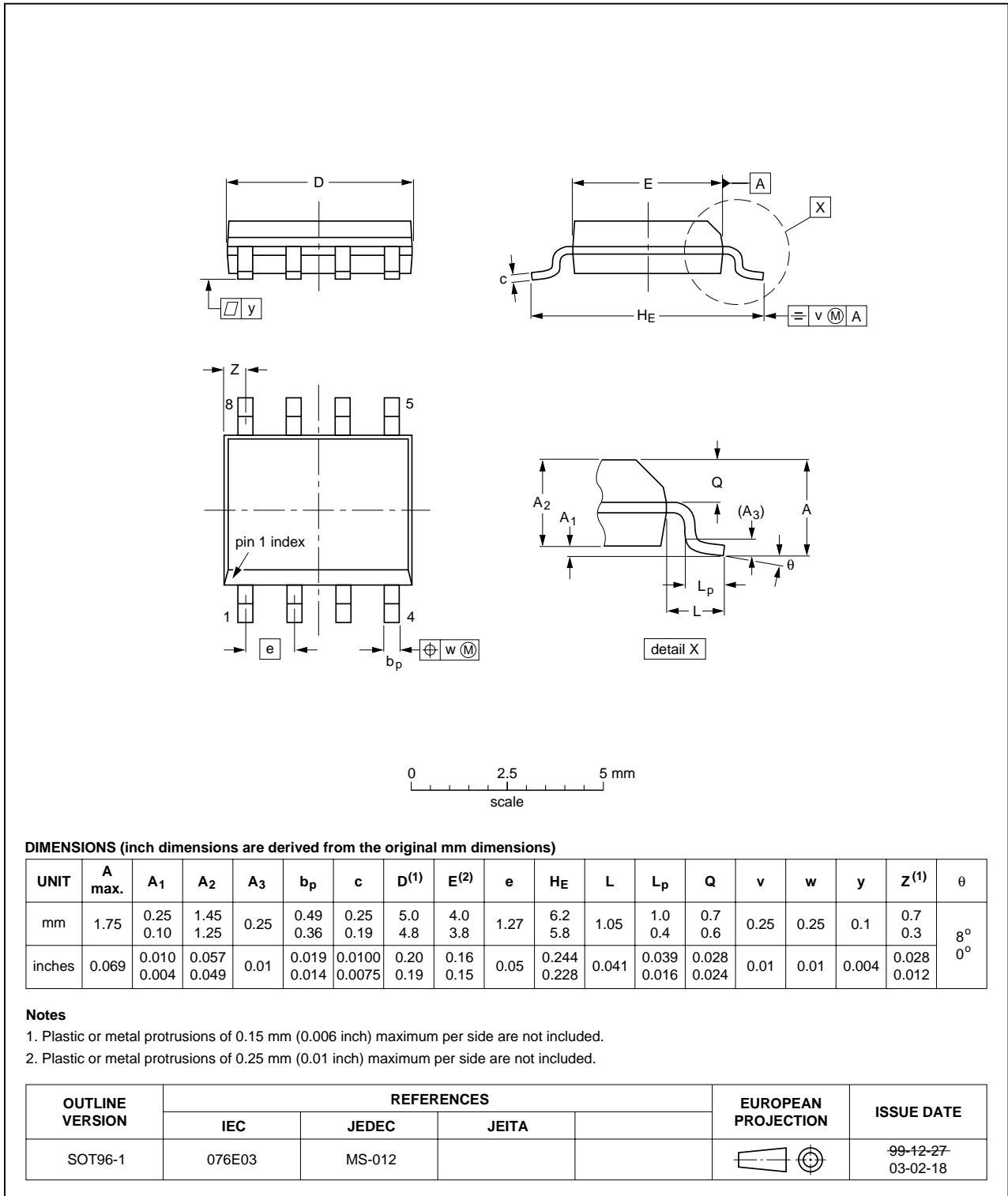


Fig 24. Package outline SOT96-1 (SO8)



TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

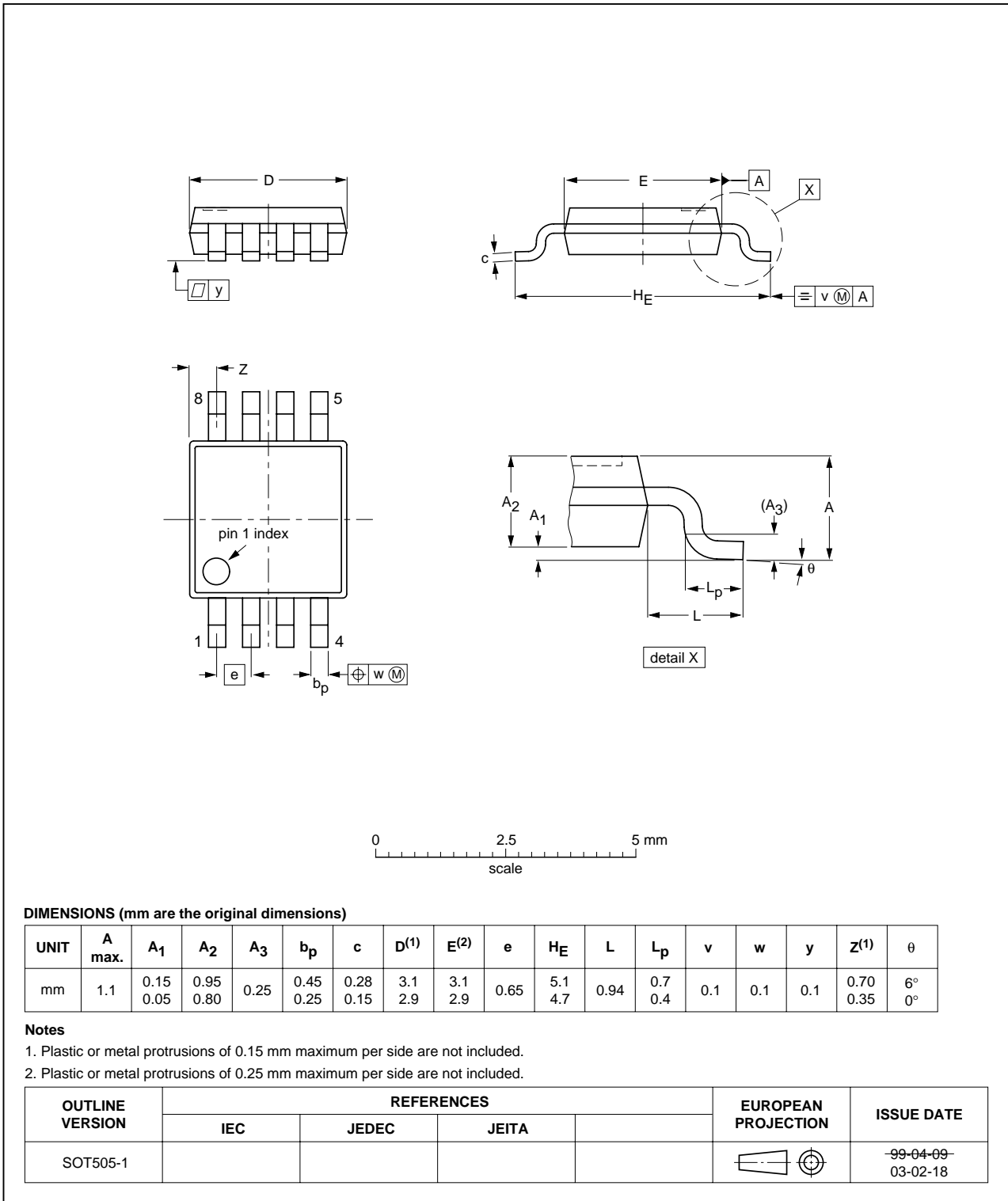


Fig 25. Package outline SOT505-1 (TSSOP8)

HVSON10: plastic thermal enhanced very thin small outline package; no leads;  
10 terminals; body 3 x 3 x 0.85 mm

SOT650-1

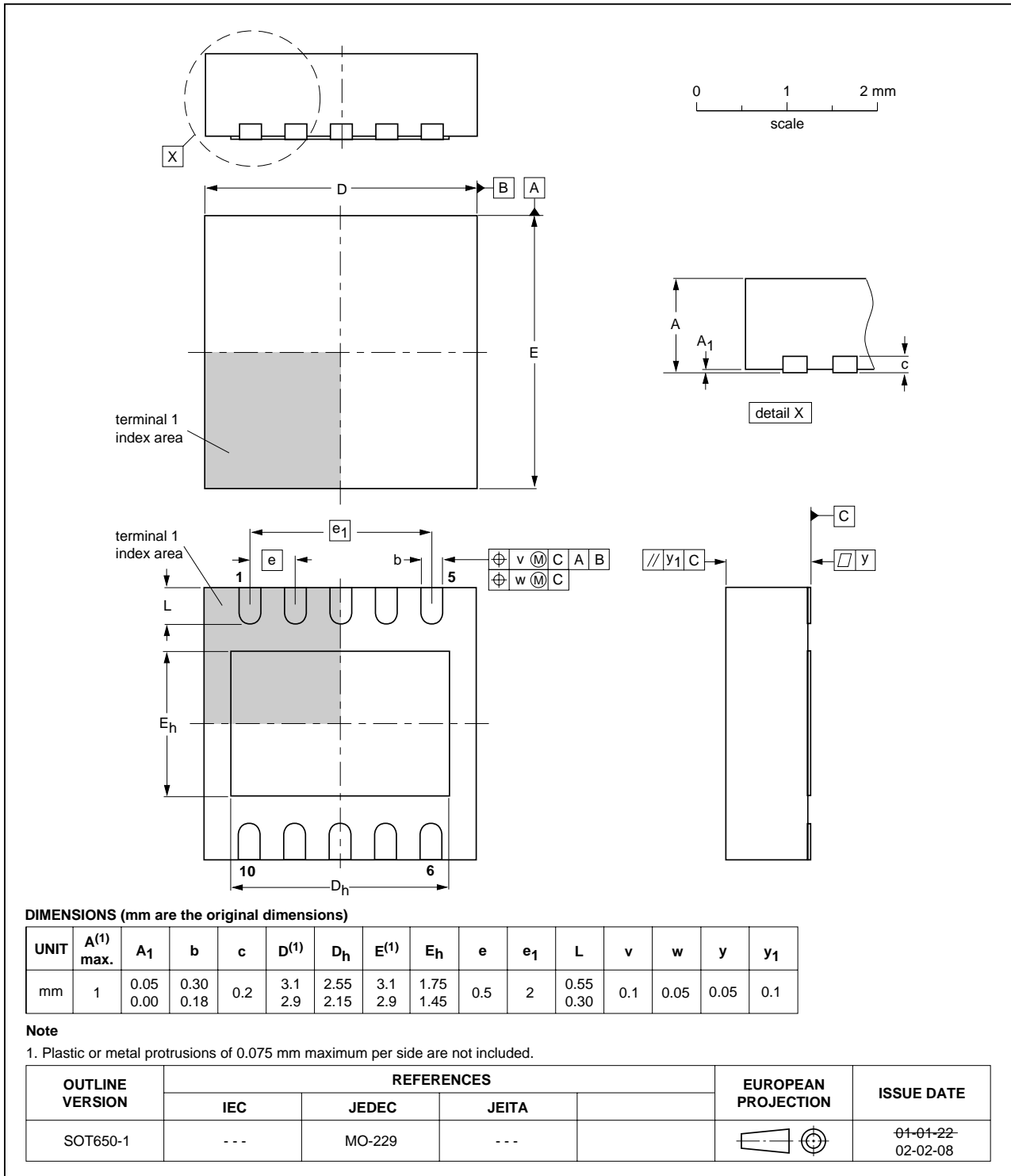


Fig 26. Package outline SOT650-1 (HVSON10)

## 14. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A* and/or *IEC61340-5*.

## 15. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 27](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 29](#) and [30](#)

**Table 29. SnPb eutectic process (from J-STD-020C)**

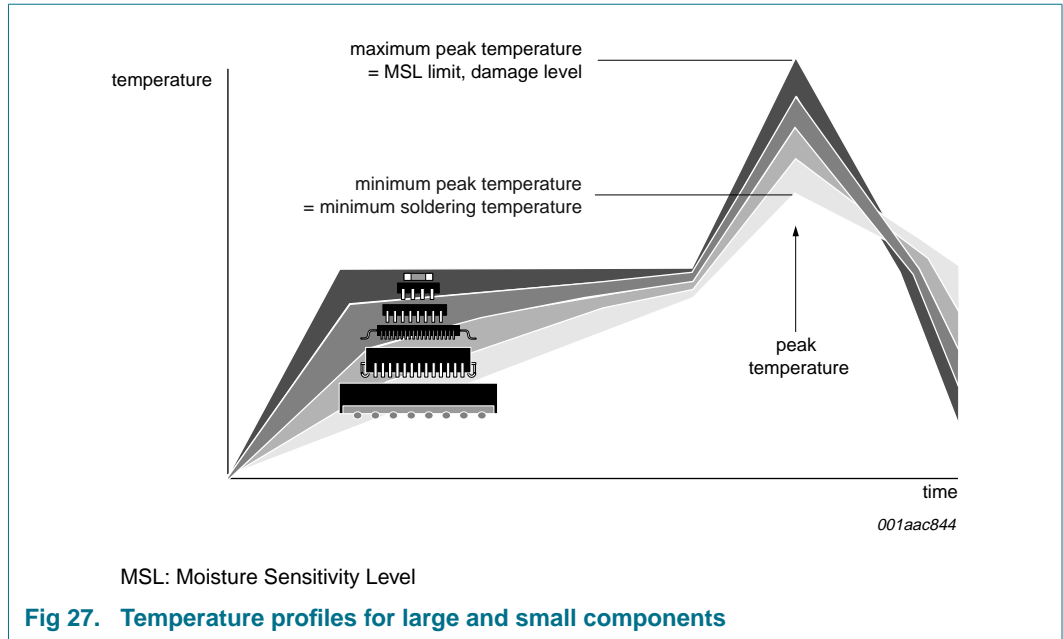
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 30. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 27](#).



For further information on temperature profiles, refer to Application Note AN10365 "Surface mount reflow soldering description".

## 16. Revision history

**Table 31. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8563_6	20080221	Product data sheet	-	PCF8563_5
Modifications:	<ul style="list-style-type: none"> <li>• Register names modified in <a href="#">Figure 1</a> and various tables.</li> <li>• <a href="#">Figure 17</a>, <a href="#">Figure 18</a> and <a href="#">Figure 19</a>: corrected the unit on the vertical axis.</li> </ul>			
PCF8563_5	20070717	Product data sheet	-	PCF8563-04
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Quick reference data table removed to comply with guidelines.</li> <li>• Table 3: Table 3 and Table 4 combined in one table.</li> <li>• Section 4: added topside mark.</li> <li>• Section 4: added HVSON10 package.</li> </ul>			
PCF8563-04 (9397 750 12999)	20040312	Product data	-	PCF8563-03
PCF8563-03 (9397 750 11158)	20030414	Product data	-	PCF8563-02
PCF8563-02 (9397 750 04855)	19990416	Product data	-	PCF8563_N_1
PCF8563_N_1 (9397 750 03282)	19980325	Objective specification	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 19. Contents

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